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Effect of Growth Rate and Wafering on Residual Stress of Diamond Wire Sawn Silicon Wafers

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Abstract

The mechanical integrity of photovoltaic (PV) silicon wafers is critical to avoid failure during solar cell manufacturing. Residual stress present in wafers affects mechanical integrity. Residual stresses are generated during solidification of ingots and during the wafering or wire sawing process used to produce silicon wafers. In this paper, the residual maximum shear stress in diamond wire sawn photovoltaic multi-crystalline silicon wafers corresponding to different crystal growth rates and their pre-and post-etched conditions are analyzed. The full-field residual stress distributions in the wafers are measured using near infra-red transmission birefringence polariscopy. Results show that wafers corresponding to the high crystal growth rate are characterized by larger residual maximum shear stress. As the growth rate increases to two times the standard growth rate, the average residual stress increases by 43%. The increase in residual stress in the high growth rate wafers is attributed to the interaction of abrasives with more grain boundaries present in these wafers. Etching results in lower residual stress for all growth rates and ingot locations.

Keywords: diamond wire sawing, multi-crystalline silicon, residual stress

1 Introduction

The high cost of photovoltaic solar cells is a significant barrier to their widespread adoption as a renewable energy alternative to conventional energy sources. Photovoltaic solar cells are built on crystalline silicon wafers, which are used as substrates. Silicon wafers are usually manufactured by

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slicing of ingots using either a loose abrasive slurry (LAS) or a fixed abrasive diamond wire sawing (DWS) process (HJ Möller, 2004). The recently published international technology roadmap for photovoltaics (ITRPV, 2014) reported a shift from LAS to DWS for manufacturing silicon wafers. DWS is characterized by several advantages over LAS, such as increased material removal rate and lower material loss due to the smaller kerf (HJ Möller, 2004). Moreover, DWS is environmentally friendly compared to slurry sawing because it enables recycling of expensive silicon particles. To reduce material cost, thinner wafers can be used. However, thinner wafers can lead to higher mechanical failure rates and therefore lower production yields unless they have higher mechanical strength. The fracture strength of silicon wafers is impacted by residual stress produced by the crystal growth (e.g. casting) and wire sawing processes. Thus, it is important to measure and understand residual stress in sliced silicon wafers. It should be noted that residual stresses are a significant factor in wafer breakage during handling and processing of silicon wafers during manufacturing of solar cells.

Multi-crystalline silicon is much cheaper than mono-crystalline silicon (HJ Möller et al., 2005). However, multi-crystalline wafers are known to be weaker than mono-crystalline wafers. Mechanical strength of multi-crystalline silicon wafers have been observed to depend on the grain size, with wafers having larger grains and fewer grain boundaries exhibiting higher strength (VA Popovich et al., 2010). This is because grain boundaries in silicon are sources of defects and tend to decrease the wafer strength. The mechanical strength of multi-crystalline silicon wafers is also influenced by local properties related to the microstructure of the material (S Wurzner et al., 2010). Residual stresses are created in the by the steep thermal gradients present during solidification and by microstructure dependent defects such as grain boundaries, inclusions, and dislocations (V Ganapati et al., 2010, A Kumar, , Skenes, K., Prasath, R.G.R., Yang, C., Melkote, S.N., Danyluk, S., 2013). Prior work has found the maximum residual stresses in multi-crystalline wafers to be associated with grain/twin boundaries (MC Brito et al., 2005, M Fukuzawa et al., 2010).

Apart from residual stresses due to solidification, the wire sawing process also introduces residual stress in the wafer. Diamond wire sawing involves “ductile grooving” and “brittle chip-off” as the main material removal mechanisms (E Cai et al., 2011). Silicon is known to undergo pressure-induced phase transformation (JZ Hu et al., 1986), which makes ductile material removal possible under controlled cutting conditions (TG Bifano et al., 1991). Prior work found that ductile cutting of silicon depends on machining parameters like the tool edge radius, the cutting edge angles, and the depth of cut (R Komanduri et al., 2001, X Li et al., 2010) The mechanism of interaction of abrasives with brittle substrates has been studied previously (R Komanduri, 1996, R Komanduri et al., 1997, C Evans et al., 2003). Machining parameters like the rake angle, the cutting edge angle, and the undeformed chip thickness can influence the conditions required for ductile material removal (J Yan et al., 2001). Scratching experiments in silicon, which simulate the cutting of silicon in DWS, have demonstrated the effect of hydrostatic pressure on ductile mode removal of silicon (M Yoshino et al., 2001). The stress induced phase transformation and metallization of silicon is accompanied by plastic deformation, which can give rise to residual stresses.

It is clear from prior literature that residual stresses in diamond wire sawn multi-crystalline silicon wafers are created in the bulk during solidification and are manifested in the wafer surface after wire sawing. Thus, there is a need to measure the residual stresses in sliced silicon wafers and to understand the effect of prior processing, which forms the motivation of our study. In this paper, we investigate the effect of growth rate and wire sawing (or wafering) on residual stresses present in multi-crystalline silicon wafers.

Methods available to measure residual stresses include x-ray diffraction (XRD), micro-Raman spectroscopy, Moire´ interferometry, transmission electron microscopy (TEM), and digital photoelasticity. Of these methods, we use the method of near-infrared (NIR) transmission photoelasticity for its non-contact nature, simplicity and lower cost. NIR photoelasticity based polariscopy is an optical method, which generates information of principal stress difference

(isochromatic) and principal stress direction (isoclinic) in the form of fringe contours. Prior work by the Danyluk group has developed the experimental setup needed for this measurement approach over a number of studies (T Zheng and S Danyluk, 2001, S He et al., 2004). Recently, this group has demonstrated the effectiveness of the ten-step phase shifting technique compared to other techniques for accurate determination of the photoelastic parameter, which is used to measure the residual stress (RGR Prasath et al., 2013). The current experiment setup uses the ten-step phase shifting method to measure the spatial distribution of through-thickness in-plane residual shear stresses in thin silicon wafers (K Skenes et al., 2014, K Skenes, 2014).

2 Experiments

In our experiment, we used 156 x 156 mm, 200~210 μm thick diamond wire sawn multi-crystalline silicon wafers, taken from ingots solidified at two different growth rates. Growth rates used are the standard growth rate (denoted by 1X) used in casting of multi-crystalline silicon ingots and twice the standard growth rate (denoted by 2X). We refer to the two cases as low and high growth rates, respectively. For each growth rate, wafers were taken from the edge and interior of the ingot to understand the differences between the two ingot locations, which are usually characterized by differences in temperatures during solidification.

Figure 1 shows a schematic of the experimental setup for the NIR transmission polariscopy technique, which is based on residual stress-induced birefringence phenomenon. The setup uses a broadband light source consisting of a tungsten filament lamp. Next in the light path, there is a NIR filter and polarizer, an input quarter wave plate, a collimating lens, the silicon wafer sample, another collimating lens, an output quarter wave plate, an analyzer, and the camera. The images obtained from this setup were recorded with a Canon EOS 50D digital single lens reflex camera with a resolution of 4752 x 3168 pixels and equipped with a 750nm low-pass filter.

The transmitted intensity captured by the camera depends on the residual stress in the wafer. Ten images at different optical settings, whose details can be found elsewhere (K Skenes et al., 2014), are recorded. The recorded images are processed using the software developed in-house. The software computes the distribution of maximum residual shear stress in the wafer using a ten-step phase shifting method (RGR Prasath et al., 2013). The technique of phase shifting balances measurement accuracy and efficiency. Using this method, the pixel-by-pixel principal stress difference, which is related to the maximum shear stress, in the whole wafer is obtained. Since the technique is based on light transmission through the thin wafer sample and it assumes the thin sample to be in a state of plane stress, the maximum residual shear stress obtained at each point in the wafer represents an average value over the entire wafer thickness.

Some researchers have used a six-step phase shifting technique to measure the residual stress in edge-defined film fed growth (EFG) silicon wafers (MC Brito et al., 2005). Other groups have used the infrared birefringence imaging (IBI) technique to calculate the internal stresses in multi-crystalline silicon wafers (V Ganapati et al., 2010).

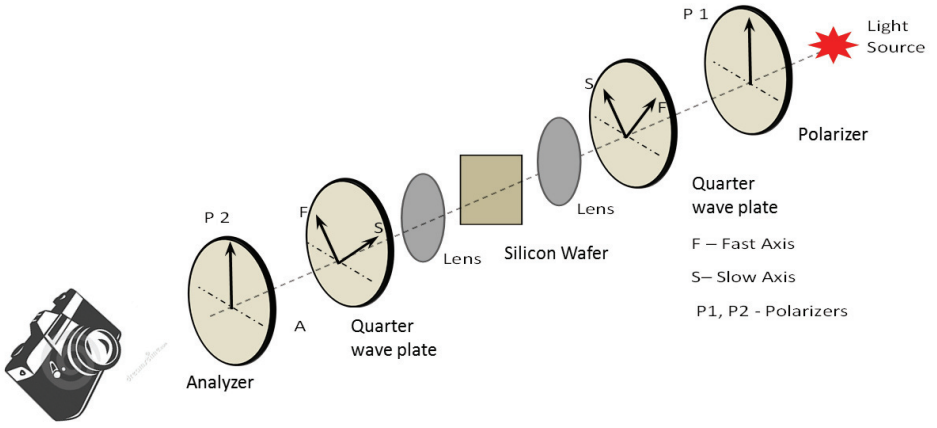


Figure 1: Schematic of NIR transmission polariscopy experimental setup.

The stress optic law is used to determine the maximum residual shear stress from the phase retardation measurements at each point in the wafer:

$$\tau_{max} = |\sigma_1 - \sigma_2| = \frac{\lambda\delta}{2\pi tC}$$

where δ is the relative retardation, λ is the wavelength of light used, C is the relative stress-optic coefficient, and t is the sample thickness. The relative retardation is obtained from the phase-stepping algorithm mentioned earlier, and the other terms of the equation are known *apriori*.

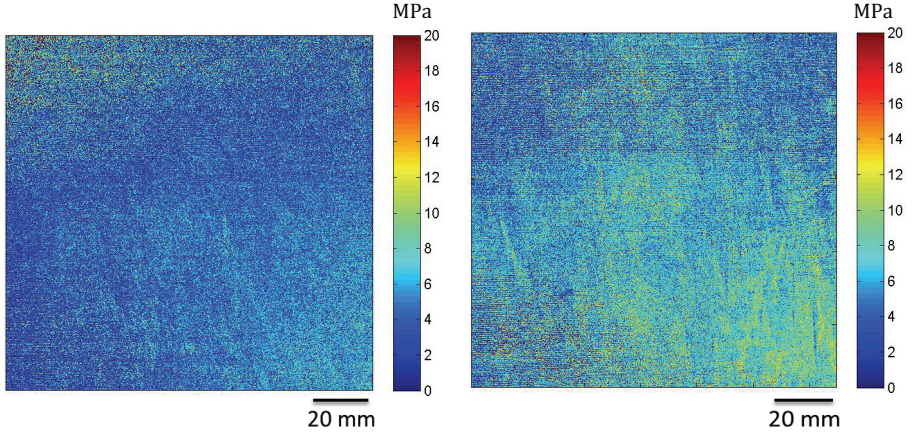
The wafers were first evaluated by the NIR polariscopy technique in their as-sawn condition. Next, the wafers were etched 5 μm on each side to remove the sawing induced damage layer on the surface using a standard industrial etching process. The residual stress distributions in the etched wafers were re-measured. It should be noted that the NIR polariscopy technique is a transmission based residual stress measurement method, which yields through-thickness residual stresses and not surface stresses.

Image processing software including ImageJ and JMicroVision were used to determine the grain sizes and the number of grains per unit area.

3 Results and Discussion

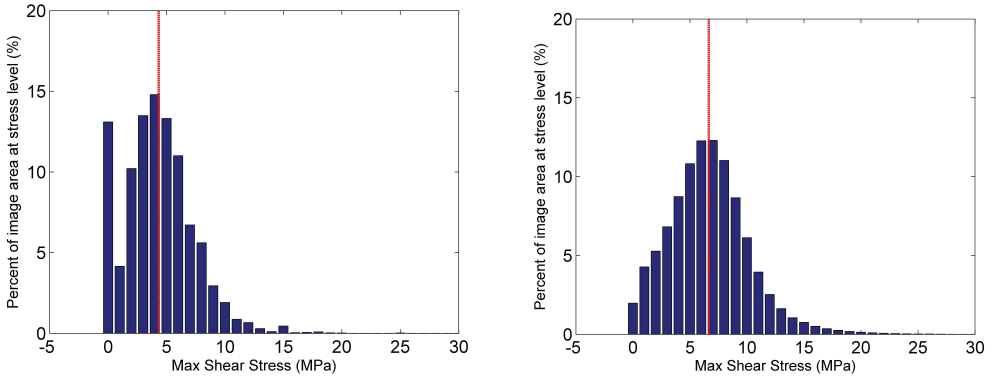
Full-field residual maximum shear stress maps obtained over the entire spatial domain of the wafer (156 mm X 156 mm) for the low and high growth rate wafers taken from the interior of the ingot are shown in Figure 2. In this paper, the term residual stress refers to the maximum shear stress or the principal stress difference. To understand the variation of residual stress within the measured area of a particular growth rate wafer, we plotted the histogram (see Figure 3) using a bin size of 1 MPa. The average or mean value was also plotted on the same graph as seen in the figure. If we consider stress level < 1 MPa, the low growth rate wafer has about 20% percent of the total area at that level, whereas the high growth rate case has only 5% of the total area. If we consider a residual stress level of 5-7 MPa, the standard or low growth rate wafer has about 25% of the total area, whereas the high growth rate wafer has about 40% of the total area at that level. Note that the total areas considered for both wafers are equal. Comparison of the average residual stress over the whole wafer reveals that the standard growth rate wafers exhibit a lower average residual stress of 4.3 MPa, compared to 6.7 MPa in the higher growth rate wafers. The RMS value of residual stresses was computed and found to be 5.3 MPa for the low growth rate wafer versus 7.5 MPa for the high growth

rate wafer. The standard deviation of the residual maximum shear stresses within the wafer shown here was 2.9 MPa for the low growth rate wafer versus 3.5 MPa for the high growth rate wafer. This indicates the point-to-point variation is more for the high growth rate case than the low growth rate case. Note that both wafers compared are extracted from the interior of the ingot. Three wafers for each growth rate were evaluated, but only one representative result per case is shown here.



(a) (b)

Figure 2. Spatial distributions of full-field residual maximum shear stress in multi-crystalline silicon wafers from the interior of the ingot: (a) low (1X) growth rate, and (b) high (2X) growth rate.

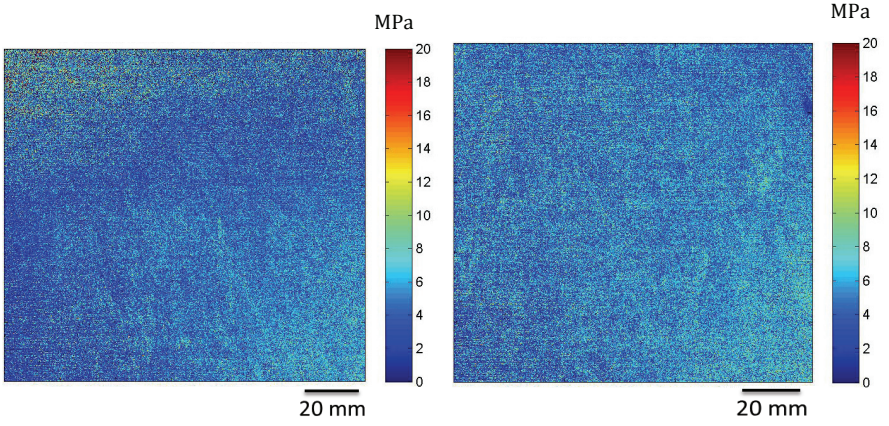


(a) (b)

Figure 3. Histograms showing the distributions of full-field residual maximum shear stress in wafers from the interior of the ingot: (a) low (1X) growth rate, and (b) high (2X) growth rate. The red line indicates the mean stress.

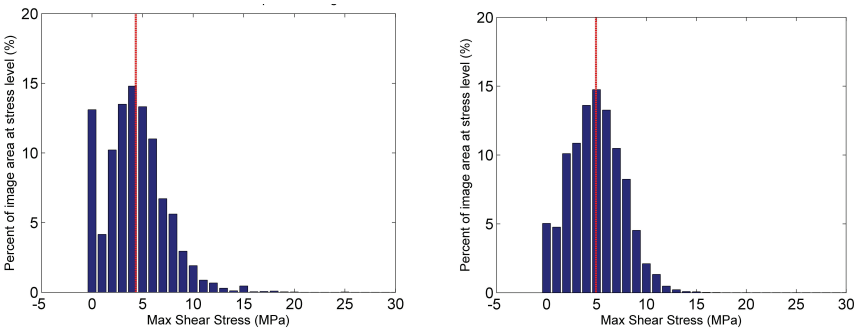
The residual maximum shear stress distribution for the low growth rate wafers taken from the edge and interior of the ingot are shown in Figure 4. The histograms for these two cases are shown in Figure 5. Comparison of the average values of residual stress over the whole area does not reveal significant difference between the interior (mean: 4.3 MPa, RMS: 5.2 MPa) and edge (mean: 4.9 MPa, RMS: 5.6 MPa), respectively. The standard deviations of the residual stress values within the two wafers were 2.9 MPa and 2.6 MPa, respectively. However, the histogram shows some differences. By

comparing Figure 5(a) and 5(b), we observe ~ 1 MPa level of stress over a large percentage of the wafer taken from the ingot's interior compared to the edge. We attribute this to the less severe temperature gradients in the interior of the ingot during solidification, leading to lower residual stresses in the interior wafer.



(a) (b)

Figure 4. Spatial distributions of full-field residual maximum shear stress in low growth rate wafers from: (a) interior, and (b) edge of ingot.

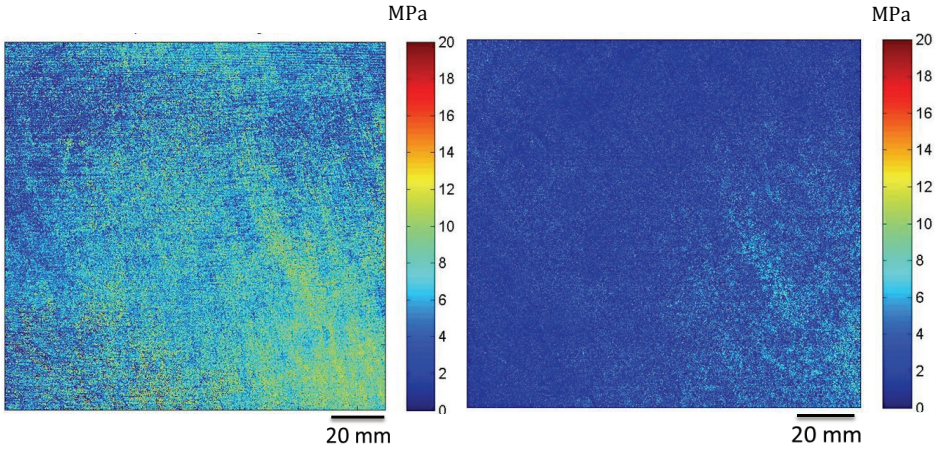


(a) (b)

Figure 5. Histograms showing the distributions of full-field residual maximum shear stress in low growth rate wafer from: (a) interior, and (b) edge of ingot. The red line indicates the mean stress.

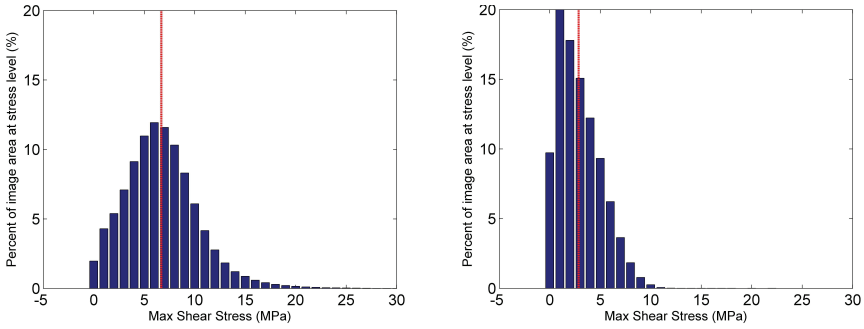
The spatial distribution of the residual maximum shear stress for the same wafer before and after etching are shown in Figure 6, where the residual stress maps show an overall decrease. Figure 7 shows the histograms of the residual maximum shear stress before and after etching. Before etching, most of the wafer area had residual stress levels ~5 MPa but after etching the stress levels decrease significantly with most of the area (> 20%) exhibiting ~1-2 MPa and a small area of the wafer exhibiting stresses > 5 MPa. The histogram plot for the post-etch condition has its Y-axis limit set at 20% for consistency with the other plots. Thus, etching removes the damaged surface layer in the as-cut wafers and lowers the residual maximum shear stress. Since the polariscopy method gives us through-thickness stresses, the stress observed after etching is indicative of the residual stresses present in the wafer bulk. Taking the average value of residual stress over the entire wafer area, we observe that there is a 40% reduction in the average residual stress in the post-etch case compared to

the pre-etch case (for the same growth rate and location in ingot). Wafers belonging to the other groups also showed similar pre- and post-etching trends.



(a) (b)

Figure 6. Spatial distributions of full-field residual maximum shear stress in a high growth rate multi-crystalline silicon wafer: (a) before, and (b) after etching (representative cases shown). The wafer is from the edge of the ingot.



(a) (b)

Figure 7. Histograms showing the distributions of full-field residual maximum shear stress of a high growth rate wafer: (a) before, and (b) after etching (representative cases shown). The red line indicates the mean stress. The wafer is from the edge of the ingot.

A comparison of the full-field residual stresses averaged over the whole wafer surface for all cases of growth rate and ingot location is shown in Figure 8.

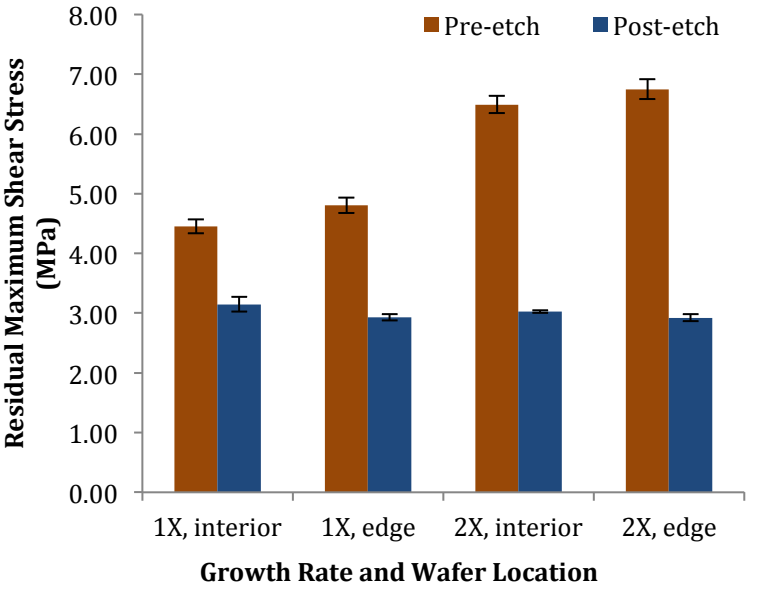


Figure 8. Residual stress, averaged over the whole wafer, for the different growth rates and locations of the ingot.

It can be seen from Figure 8 that, prior to etching, the average residual maximum shear stress is consistently larger in the higher growth rate wafer. A probable reason for this observation is the increased interaction of the diamond abrasives during wire sawing with more grains and grain boundaries present in the higher growth rate wafer. The high growth rate ingot (and hence, wafer) is characterized by faster cooling rates during solidification, and therefore has smaller and more grains than the low growth rate wafer. Hence, more interaction of the diamond abrasives with grain boundaries is expected, leading to higher residual stress due to sawing in the high growth rate wafer. In support of our hypothesis, we analyzed the grain sizes in the wafers for the two growth rates taken from the interior of the ingot using the multiple lines intercept counting method (ASTM-E112-13, 2004, ASTM-E1382, 2015, M Schumann et al., 2011). In this method, multiple straight lines are drawn across the image of the wafer and the number of intersections of each line with the grain boundaries is counted. By dividing the length of the line by the number of grain boundaries crossed, an average grain size is obtained. We divided the whole wafer by 7 horizontal lines and 7 vertical lines, and determined the average grain size for each line, as shown in Figure 9. The corresponding average grain size statistics are shown in Figure 10. It can be seen that the higher growth rate wafer has smaller grains and more grains within a given area than the lower growth rate wafer.

In addition, it can be seen from Figure 8 that the average residual shear stresses in the wafers taken from the edge of the ingot and prior to etching are slightly higher than in the low growth rate wafers. However, the post-etch results show that residual stresses are almost the same for all growth rates and ingot locations. This observation is contrary to what is expected. By way of solidification alone, the higher growth rate material is expected to have faster cooling rates and correspondingly higher residual stresses, especially at the edge of the ingot. Interestingly however the post-etch results do not exhibit any significant differences in the average residual shear stress either as a function of growth rate or ingot location. Further investigation is required to understand this result. However, for all cases, the average residual stresses are lower after etching.

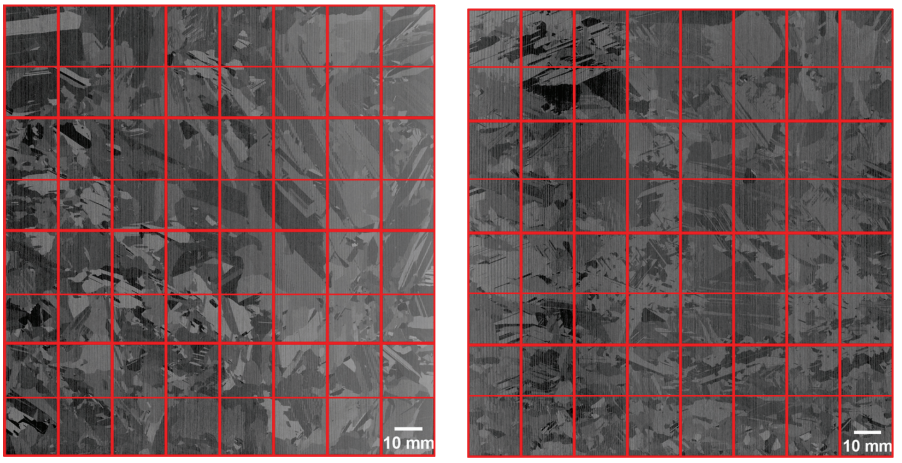


Figure 9. Grain size estimation using line intercept method for: (a) low (1X) growth rate wafer, and (b) high (2X) growth rate wafer. Both wafers are from the interior of the ingot.

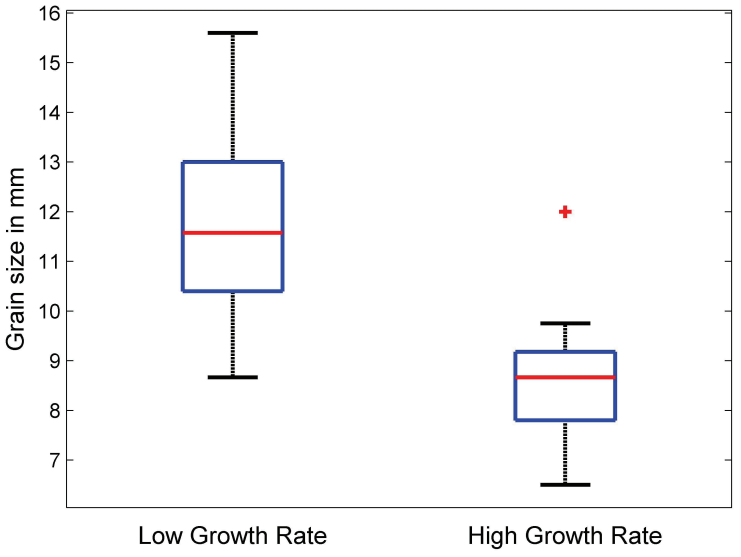


Figure 10. Box plot of grain size differences between the two growth rates; both wafers are from the interior of the ingot.

4 Conclusions

The paper analyzed the effects of crystal growth rate and location of wafer in the ingot on the residual maximum shear stress in fixed abrasive diamond wire sawn multi-crystalline silicon wafers. Results revealed differences in the residual stress for different growth rates and ingot locations prior to saw damage removal etch. It is hypothesized that the differences in the residual stresses in the high growth rate case (irrespective of wafer location) are due to increased interaction of abrasive grits with the silicon grain boundaries, which is impacted by the growth rate. Higher growth rate yields smaller grains in a given area of the wafer compared to the low growth rate case. Thus, there are more grain boundaries at a higher growth rate, and they interact with the abrasive during the wire sawing process, thereby increasing the residual stresses. There are some differences in the spatial distribution of residual maximum shear stress in wafers at the interior of ingot versus at the edge. Prior to etching, the average residual maximum shear stress is slightly greater in the wafers at the edge of the ingot compared to those in the interior of the ingot, irrespective of the growth rate. While etching of the saw damage layer lowers the residual stress in all cases, no differences in the growth rate or ingot location are evident in the post-etched wafers.

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